

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Bruce B. DORIS, *et al.*

Docket No.: FIS920030247US1

Appln. No. : 10/605,672

Group Art Unit: 2812

Filed : October 16, 2003

Examiner: ISAAC, Stanetta D.

For : **HIGH PERFORMANCE STRAINED CMOS DEVICES**

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
U.S. Patent and Trademark Office  
Customer Service Window, Mail Stop AF  
Randolph Building  
401 Dulany Street  
Alexandria VA 22314

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, and supplemental to the Information Disclosure Statement filed on October 17, 2005, applicant respectfully brings the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. The Supplemental Information Disclosure Statement is being filed concurrently with a Request for Continued Examination (RCE).

Further to the U.S. Patent and Trademark Office's decision to waive the requirement under 37 C.F.R. § 1.98 (a)(2)(i), copies of the U.S. patents and U.S. published patent applications are not enclosed herewith. However, if any copies are needed, the Examiner is respectfully requested to contact the undersigned.

Applicants respectfully request that the Examiner consider the materials cited and indicate such consideration by appropriately initialing the enclosed PTO-1449 Form and including a copy of the initialed form in the next official communication.

Should there be any questions concerning this application, the Examiner is invited to contact the undersigned at the below listed telephone number.

Respectfully submitted,  
Bruce B. DORIS, *et al.*

A handwritten signature in black ink, appearing to be 'A. Calderon', written over a horizontal line.

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FORM PTO-1449	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. P27161	Application No. 10/605,672
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use several sheets if necessary)		Applicant Bruce B. DORIS <i>et al.</i>	
		Filing Date October 16, 2003	Group 2812

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	NO
		JP 64-76755	3-22-1989	Japan				X

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

\*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449		U.S. Department of Commerce Patent and Trademark Office		Atty. Docket No.		Application No.	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use several sheets if necessary)				Applicant			
				Filing Date		Group	
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
<b>FOREIGN PATENT DOCUMENTS</b>							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
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		G. Zhang, et al., "A New 'Mixed-Mode' Reliability Degradation Mechanism in Advanced Si and SiGe Bipolar Transistors." IEEE Transactions on Electron Devices, vol. 49, no. 12, December 2002, pp. 2151-56.					
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EXAMINER				DATE CONSIDERED			
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